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1. (amended) A method for making a programmable resistance memory element, comprising:

providing a conductive material;

forming a sidewall spacer [over] on top of [a portion of] said conductive material;

removing a portion of said conductive material to form a [raised] protruding portion [extending from] of said conductive material under said spacer; and

forming a programmable resistance material adjacent to at least a portion of said [raised] protruding portion.

6. (amended) The method of claim 5, wherein said forming said sidewall surface step, comprises:

forming a [forth] fourth layer over said second layer;

removing a portion of said [forth] fourth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

13. (amended) The method of claim 6, wherein said [forth] fourth layer is a photoresist.

19. (amended) A method for making a programmable resistance memory element, comprising:

providing a conductive layer;

forming a [raised] protruding portion of said conductive layer extending from an edge of said conductive layer; and

forming a programmable resistance material adjacent to at a least a portion of said [raised] protruding portion.

20. (amended) The method of claim 19, wherein said forming said [raised] protruding portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said [raised] protruding portion under said mask.

24. (amended) The method of claim 20, wherein said mask has a lateral dimension less than 1000 [Angstoms] Angstroms.

27. (amended) The method of claim 26, wherein said forming said sidewall surface step, comprises:

forming a [forth] fourth layer over said second layer;

removing a portion of said [forth] fourth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

34. (amended) The method of claim 27, wherein said [forth] fourth layer is a photoresist.

35. (amended) The method of claim 19, wherein said forming said memory material step comprises forming said memory

material adjacent to a top surface of said [raised] protruding portion.

37. (amended) The method of claim 19, wherein conductive layer is a conductive sidewall [layer] spacer or a conductive sidewall liner.

40. (amended) A method of forming a programmable resistance memory element, comprising:

providing a first dielectric layer;

forming a sidewall surface in said dielectric layer;

forming a conductive layer on said sidewall surface;

forming a second dielectric layer over said conductive layer;

[forming or exposing an edge of said conductive layer;

forming a protruding portion extending from said edge of said conductive layer; and

forming a programmable resistance material adjacent to at least a portion of said protruding portion]

forming a mask over an exposed top surface of said conductive layer;

removing a portion of said conductive layer to form a protruding portion of said conductive layer under said mask; and

forming a programmable resistance material adjacent to at least a portion of said protruding portion.

42. (amended) The method of claim [41] 40, wherein said removing step comprises etching said conductive layer.

45. (amended) The method of claim [41] 40, wherein said mask has a lateral dimension less than 1000 Angstroms.

46. (amended) The method of claim [41] 40, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

47. (amended) The method of claim 46, wherein said forming said sidewall spacer step comprises:

forming a first layer over said [edge] exposed top surface of said conductive layer;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

48. (amended) The method of claim 47, wherein said forming said sidewall surface step, comprises:

forming a [forth] fourth layer over said second layer;

removing a portion of said [forth] fourth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

55. (amended) The method of claim 48, wherein said [forth] fourth layer is a photoresist.

56. (amended) The method of claim 40, wherein said forming said programmable resistance material step comprises the steps of:

forming a third dielectric layer [on said edge and] over said [raised] protruding portion;

removing a portion of said third dielectric layer to expose a top surface of said [raised] protruding portion; and

forming said programmable resistance material over at least a portion of said top surface of said protruding portion.

58. (amended) The method of claim 57, wherein forming said conductive layer on said sidewall surface step comprises forming said conductive layer on said sidewall surface and on substantially all of said bottom surface of said opening.

63. (amended) A method for making an electrode for a semiconductor device, comprising:

providing a conductive layer; and

forming a [raised] protruding portion of said conductive layer extending from an edge of said conductive layer.

64. (amended) The method of claim 63, wherein said forming said [raised] protruding portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said [raised] protruding portion under said mask.

68. (amended) The method of claim 64, wherein said mask has a lateral dimension less than 1000 [Angstoms] Angstroms.

71. (amended) The method of claim 70, wherein said forming said sidewall surface step, comprises:

forming a [forth] fourth layer over said second layer;

removing a portion of said [forth] fourth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

78. (amended) The method of claim 71, wherein said [forth] fourth layer is a photoresist.

81. (amended) The method of claim 63, wherein conductive layer is a conductive sidewall [layer] spacer or a conductive sidewall liner.

82. (amended) A method of making an electrode for a semiconductor device, comprising:

providing a first dielectric layer;

forming a sidewall surface in said dielectric layer;

forming a conductive layer on said sidewall surface;

forming a second dielectric layer over said conductive layer;

[forming or exposing an edge of said conductive layer; and

forming a raised portion extending from said edge of said conductive layer]

forming a mask over an exposed top surface of said conductive layer; and

removing a portion of said conductive layer to form a protruding portion of said conductive layer under said mask.

84. (amended) The method of claim [84] 82, wherein said removing step comprises etching said conductive layer.

87. (amended) The method of claim [83] 82, wherein said mask has a lateral dimension less than 1000 [Angstroms] Angstroms.

88. (amended) The method of claim [83] 82, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

89. (amended) The method of claim 88, wherein said forming said sidewall spacer step comprises;

forming a first layer over said [edge] exposed top surface;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

90. (amended) The method of claim 89, wherein said forming said sidewall surface step, comprises:

forming a [forth] fourth layer over said second layer;

removing a portion of said [forth] fourth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

97. (amended) The method of claim 90, wherein said [forth] fourth layer is a photoresist.

98. (amended) The method of claim 82, [wherein said forming said programmable resistance material step comprises] further comprising the steps of:

forming a third dielectric layer [on said edge and] over said [raised] protruding portion; and

removing a portion of said third dielectric layer to expose a top surface of said [raised] protruding portion.

100. (amended) The method of claim 99, wherein forming said conductive layer on said sidewall surface step comprises forming said conductive layer on said sidewall surface and on substantially all of said bottom surface of said opening.